UNITRODE

**APPLICATION NOTE**

# PHASE SHIFTED, ZERO VOLTAGE TRANSITION DESIGN CONSIDERATIONS and the UC3875 PWM CONTROLLER

**BILL ANDREYCAK**

## ABSTRACT

*This Application Note will highlight the design considerations incurred in a high frequency power supply using the Phase Shifted Resonant PWM control technique. An overview of this switching technique including comparisons to existing fixed frequency non-resonant and variable frequency Zero Voltage Switching is included. Numerous design equations and associated voltage, current and timing waveforms supporting this technique will be highlighted. A general purpose Phase Shifted converter design guide and procedure will be introduced to assist in weighing the various design tradeoffs. An experimental 500 Watt, 48 volt at 10.5 amp power supply design operating from a preregulated 400 volt DC input will be presented as an example. Considerations will be given to the details of the magnetic, power switching and control circuitry areas. A summary of comparative advantages, differences and tradeoffs to other conversion alternatives is included.*

**UC3875 CONTROL CIRCUIT SCHEMATIC**

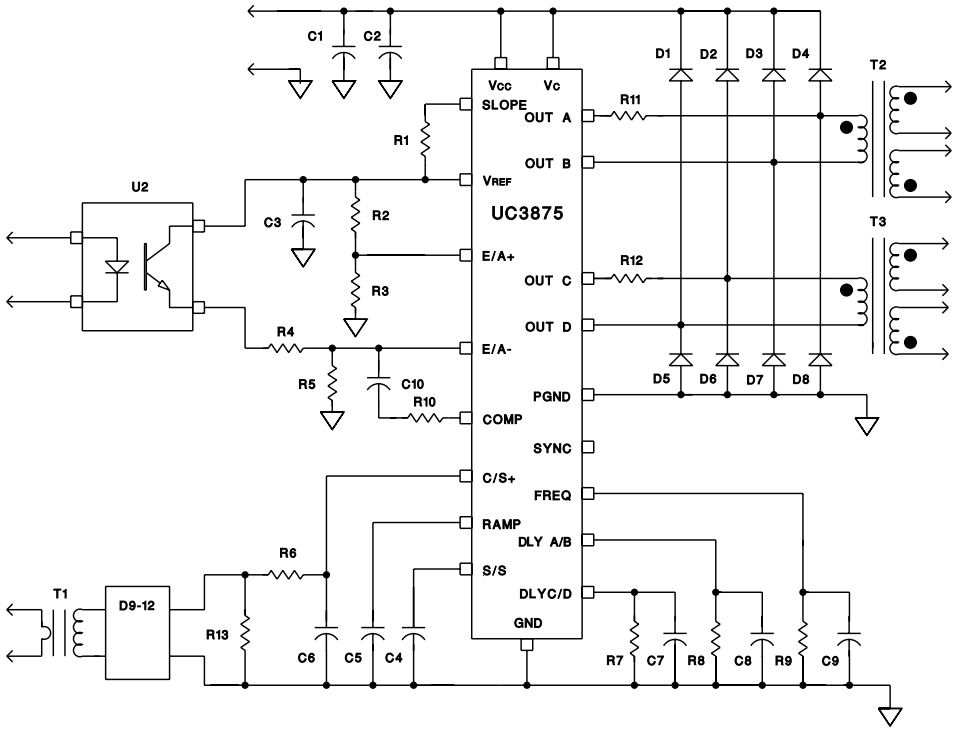


**Figure 1**

## INTRODUCTION

The merits of lossless transitions using Zero Voltage Switching techniques have already been established in power management applications. [1-5] Effects of the parasitic circuit elements are used advantageously to facilitate the resonant transitions as opposed to being dissipatively snubbed. This resonant tank functions to position zero voltage across the switching device prior to turn-on, eliminating any power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources stand to gain significant improvements in efficiency with this technique. The full bridge topology as shown in figure 2. will be the specific focus of this presentation, with an emphasis placed on the fixed frequency, phase shifted mode of operation.

**Full Bridge Topology - General Circuit**

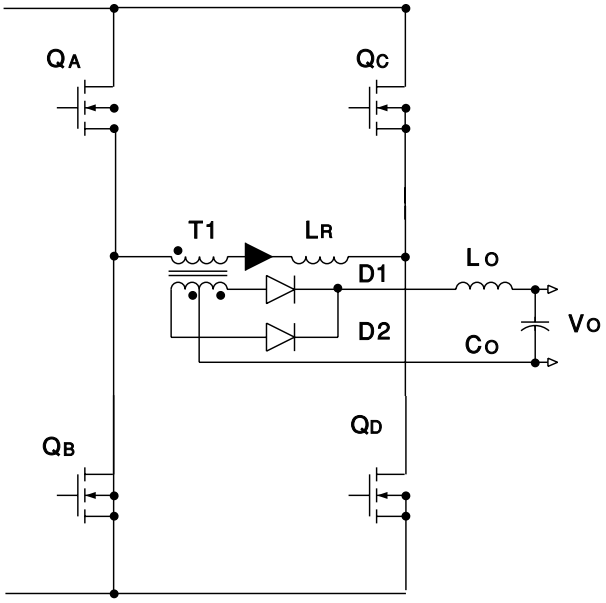


**Figure 2**

## SWITCH DRIVE COMMANDS

The diagonal bridge switches are driven together in a conventional full bridge converter which alternately places the transformer primary across the input supply, Vin, for some period of time, t(on) as shown in figure 3.

Power is only transferred to the output section during the ON times of the switches which corresponds to a specific duty cycle when operated at fixed frequency. Additionally, the complete range of required duty cycles is unique to the application, and can be estimated from the power supply input and output voltage specifications.

**Conventional Full Bridge PWM Waveforms**

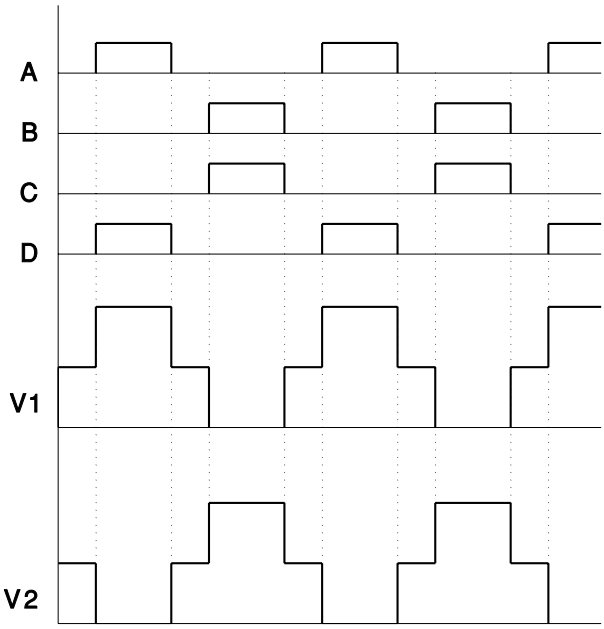


**Figure 3**

Rather than driving both of the diagonal full bridge switches together, a deliberate delay will be introduced between their turn-on commands with the Phase Shifted approach. This delay will be adjusted by the voltage loop of the control circuitry, and essentially results as a phase shift between the two drive signals. The effective duty cycle is controlled by varying the phase shift between the switch drive commands as shown in figure 4.

Unique to this Phase Shifted technique, two of the switches in series with the transformer can be ON, yet the applied voltage to the transformer is zero. These are not diagonal switches of the full bridge converter, but either the two upper or two lower switches. In this mode the transformer primary is essentially short circuited and clamped to the respective input rail. Primary current is maintained at its previous state since there is no voltage available for reset to take place. This deadband fills the void between the resonant transitions and power transfer portion of the conversion cycle. Switches can be held in this state for a certain period of time which corresponds to the required off time for that particular switching cycle.

When the correct one of these switches is later turned off, the primary current flows into the switch output capacitance (Coss) causing the switch drain voltage to resonate to the opposite input rail. This aligns the opposite switch of the particular bridge “leg” with zero voltage across it enabling Zero Voltage Switching upon its turn ON.

**Phase Shifted PWM Control Waveforms**

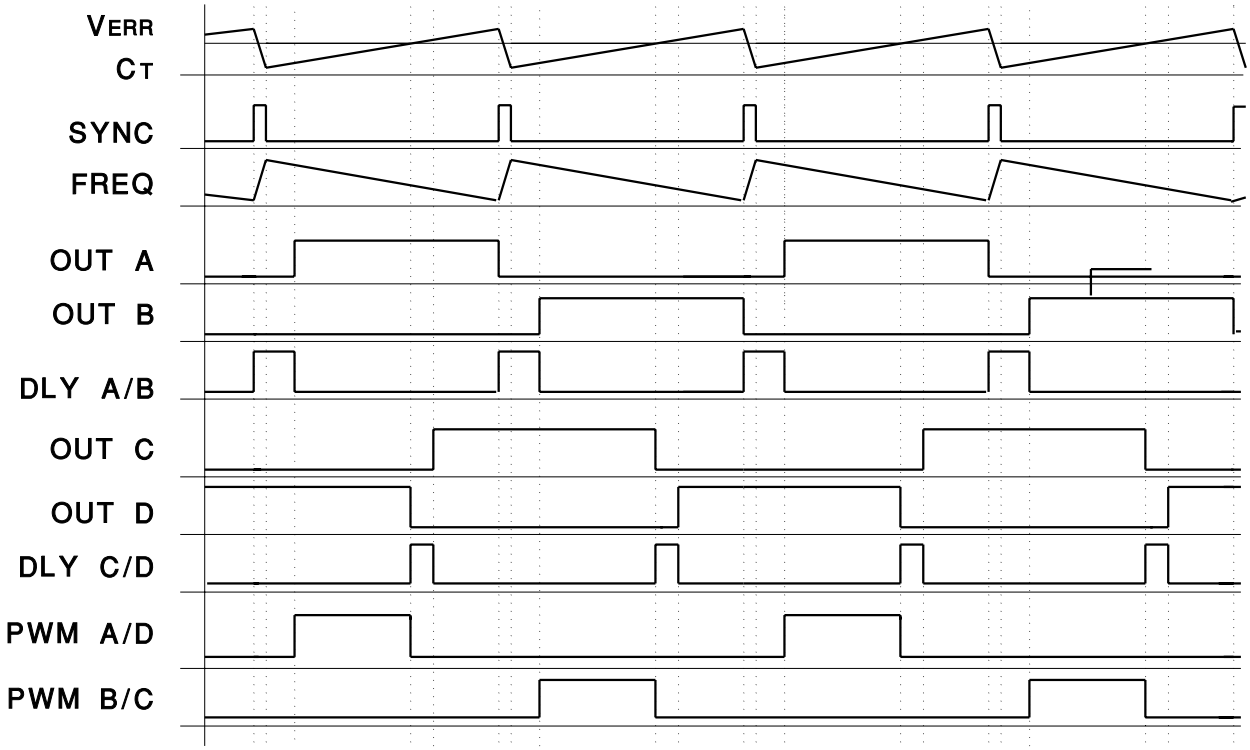


**Figure 4**

## ZVS FUNDAMENTALS

An intentional dead-time can be introduced in the power conversion cycle whereby the switch remains off and is clamped at zero voltage by the resonant tank. Rather then turn the switch on instantly when zero voltage is attained, the switch is held off while the primary current circulates into the shorted primary through the body diode and the opposite leg switch, which is still on. This off time is used to fill in the voids between the point where zero voltage has been reached where the switch needs to turned on to achieve fixed frequency operation.

Fixed frequency operation is obtainable over an identified range of input voltages and output currents. For reference purposes, the variable frequency ZVS technique has similar limitations for proper operation which occur at minimum output load and maximum input line as shown in figure 5.

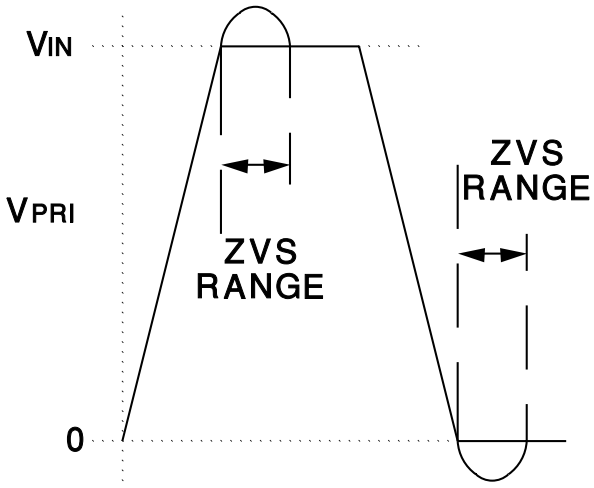


**Figure 5**

**ZVS Limitations**

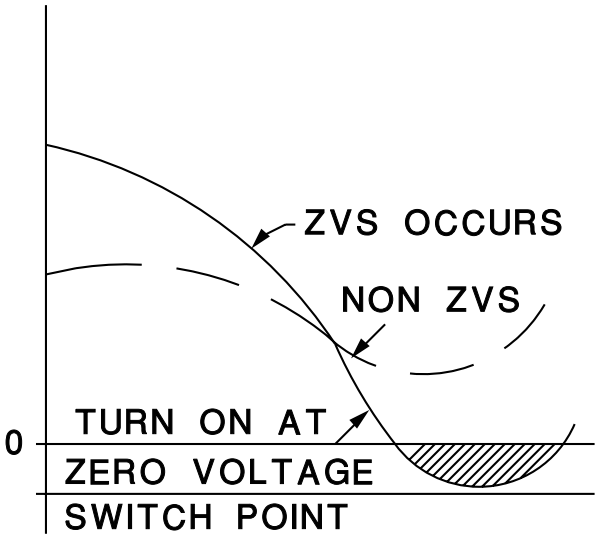


**Figure 6**

**Phase Shifted PWM Switch Orientation**

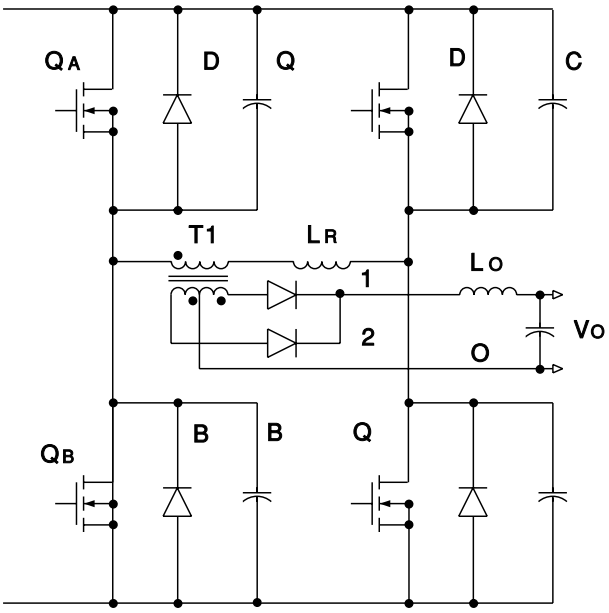


**Figure 7**

## PHASE SHIFTED FUNDAMENTALS

Switches within the Phase Shifted full bridge converter will be utilized differently than those of its nonresonant counterpart. Instrumental to this technique is the use of the parasitic elements of the MOSFET switch's constructuin. The internal body diode and output capacitance (Coss) of each device (in conjunction with the primary current) become the principal components used to accomplish and commutate the resonant transitions.

## CIRCUIT SCHEMATIC AND DESCRIPTION

Detailed operation of the Phase Shifted Converter operation will begin following a description of the circuit elements. The circuit schematic of this technique is shown in figure 7. including voltage and current designations.

The basic circuit is comprised of four switches labeled QA through QD and is divided up into two "legs", the right and left hand legs. Each switch is shown shunted by its body diode (DA through DD) and parasitic output capacitance, (CA through CD). These have been identified separately to clarify the exact elements and current paths during the conversion interval.

A detailed model of the transformer primary section is presented which separately indicates the leakage and magnetizing inductances and currents of the primary. The reflected secondary contributors to primary current are also shown for completeness, and divided into two components. The DC primary current (IP) is the secondary DC output current divided by the transformer turns ratio (N). The secondary AC current should also accounted for by multiplying the output inductance by the turns ratio squared (N^2), or dividing the secondary AC ripple current Isec(ac) by the turns ratio (N) as shown in figure 8.

**Primary Magnetic Components**

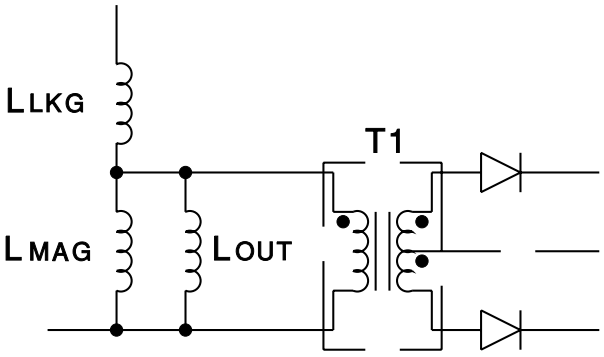


**Figure 8**

**INITIAL CONDITIONS : t = t(0)**

The description of the Phase Shifted operation will begin with the conclusion of one power transfer cycle. This occurs when the transformer had been delivering power to the load and two of diagonal switches of the converter were conducting. The initial current flowing in the primary can be designated as Ip(t(0)).

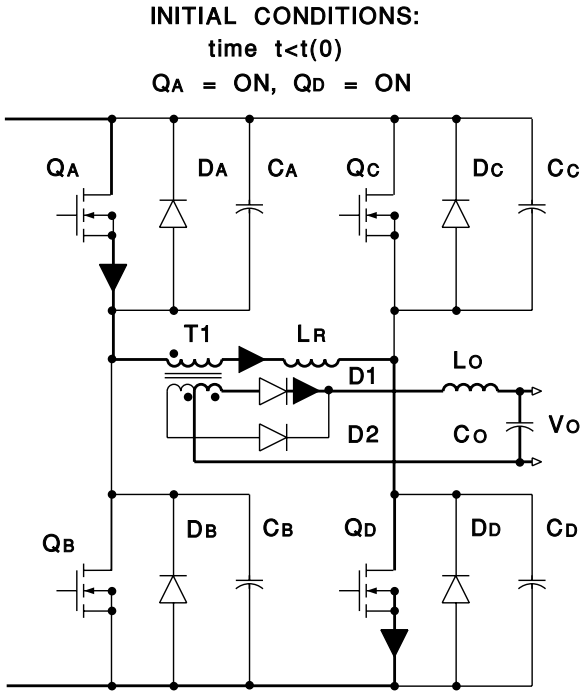


**Figure 9**

**RIGHT LEG RESONANT TRANSITION : INTERVAL: t(0) <t <t(1)**

The primary current flowing at time t(0) is equal to Ip(t(0)) and was being conducted through the diagonal set of transistors QA in the upper left hand corner of the bridge and transistor QD in the lower right. Instantly, at time t(0) switch QD is turned off by the control circuitry which begins the resonant transition of the right hand leg of the converter.

The primary current flowing is maintained nearly constant at Ip(t(0)) by the resonant inductance (Lp(res)) of the primary circuit, often referred to as the transformers leakage inductance. Since an external series inductance can be added to alter the effective leakage inductance value, this presentation will refer to the lumped sum of these inductors as the resonant inductance, Lr. In a practical application it may be difficult to accurately control the transformers leakage inductance within an acceptable ZVS range, necessitating an external “shim” inductor to control the accuracy. It’s also possible that the transformer leakage inductance can be too low to provide the desired transition times for the application so an external inductor can be introduced to modify the resonant inductance.

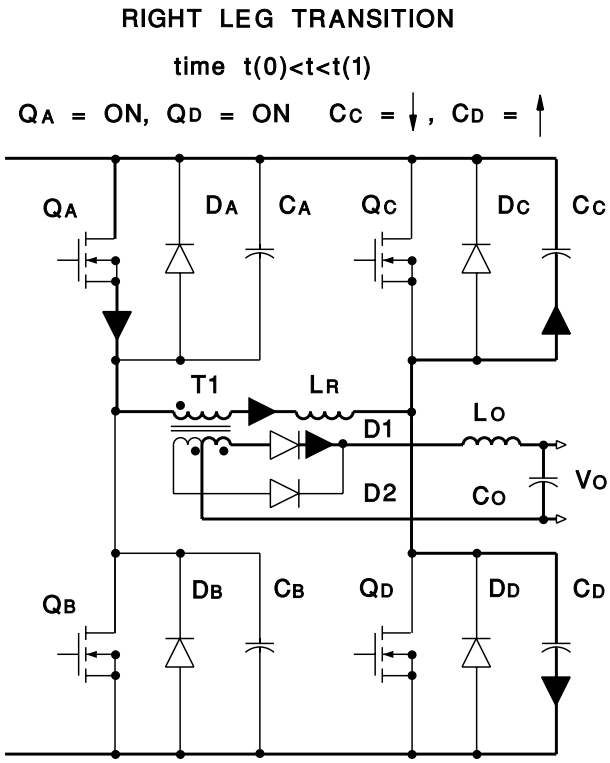


**Figure 10**

With switch QD turned off, the primary current continues to flow using the switch output capacitance, Coss to provide the path. This charges the switch capacitance of QD from essentially zero volts to the upper voltage rail, Vin+. Simultaneously, the transformer capacitance (Cxfmr) and the output capacitance of switch QC is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions switch QC with no drain to source voltage prior to turn-on and facilitates lossless, zero voltage switching.

The primary current causing this right leg transition can be approximated by the full load primary current of IP(t(0)). The small change due to the barely resonant circuit contribution is assumed to be negligible in comparison to the magnitude of the full load current.

During this right leg transition the voltage across the transformers primary has decreased fom Vin to zero. At some point in the transition the primary voltage drops below the reflected secondary voltage, Vout*N. When this occurs the primary is no longer supplying full power to the secondary and the output inductor voltage changes polarity. Simultaneously, energy stored in the output choke begins supplementing the decaying primary power until the primary contribution finally reaches zero.

Once the right leg transition has been completed there is no voltage across the transformer primary. Likewise, there is no voltage across the transformers secondary winding and no power transferred, assuming ideal conditions. Note that the resonant transition not only defines the rate of change in primary and secondary voltages dV/dt, but also the rate of change in current in the output filter network, dI/dt.

**CLAMPED FREEWHEELING INTERVAL**
**Time t(1) <t <t(2)**

Once the right leg transition is complete the primary current free wheels through transistor QA and the body diode of switch QC. The current would remain constant until the next transition occurs assuming that the components were ideal. Switch QC can be turned on at this time which shunts the body diode with the FET Rds(on) switch impedance thus lowering conduction losses. Although current is flowing opposite to the normal convention (source to drain) the channel of QC will conduct and divide the current between the switch and body diode.

**LEFT LEG TRANSITION :**
**Time t(2) <t <t(3)**

At time t(2) a residual current was flowing in the primary of the transformer which is slightly less than IP(t(0)) due to losses. Switch QC has been previously turned ON and switch QA will now be turned OFF. The primary current will continue to

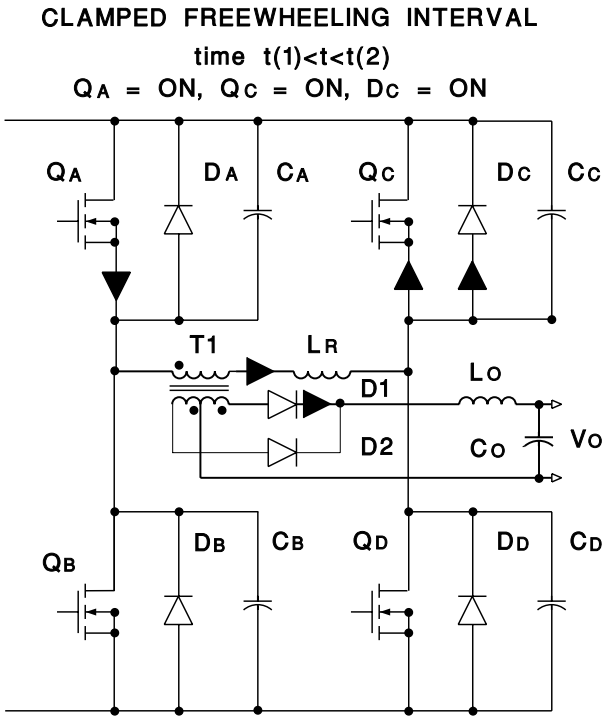


**Figure 11**

flow but the path has changed to the output capacitance (Coss) of switch QA instead of its channel. The direction of current flowing causes the drain to source voltage of switch QA to increase and lowers its source from the upper to lower rail voltage. Just the opposite conditions have occurred to switch QB which previously had the full input across its terminals. The resonant transition now aligns switch QB with zero voltage across it, enabling lossless switching to occur.

Primary current continues to flow and is clamped by the body diode of switch QB, which is still OFF. This clamping into a short circuit is a necessary condition for fixed frequency, zero voltage switching. Once switch QB is turned ON, the transformer primary is placed across the input supply rails since switch QC is already ON and will begin to transfer power. Although zero voltage switching has already been established, turning ON switch QB the instant it reaches zero voltage will cause variable frequency operation.

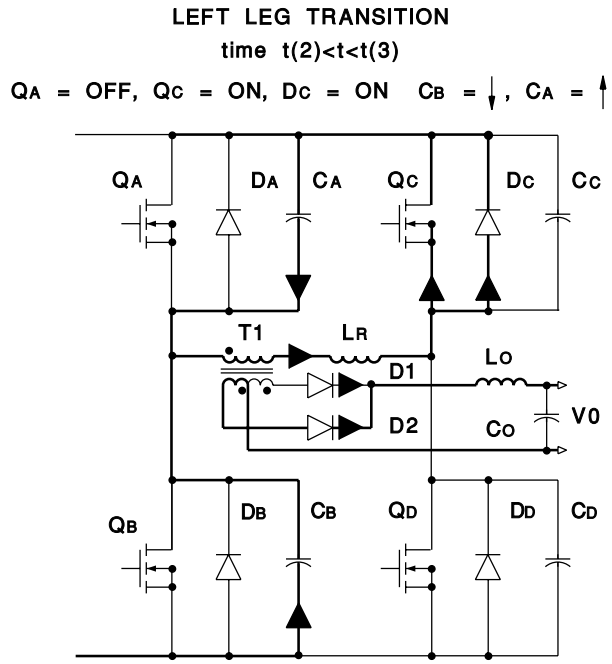


**Figure 12**

Note that this left leg transition will require more time to complete than the right leg transition. Conduction losses in the primary switches, transformer winding and interconnections result in a net DC voltage drop due to the flowing primary current. Energy stored in the series resonant inductor and magnetizing inductance is no longer ideally clamped to zero voltage. This loss, in addition to the losses incurred during the previous transition, reduce the primary current below its initial (IP(t(0)) value, thus causing a longer left leg transition time than the right leg.

Unlike conventional power conversion, one transistor in the diagonal pair of the phase shifted full bridge converter is ON just before power is transferred which simplifies the gate drive. An additional benefit is realized by designating these commutating switches as the high side switches of the converter, usually far more difficult to drive than their lower side counterparts.

**POWER TRANSFER INTERVAL**
**Time t(3) <t <t(4)**

This interval of the phase shifted cycle is basically identical to that of conventional square wave power convesion. Two diagonal switches are ON which applies the full input voltage across the transformer primary. Current rises at a rate determined by Vin and the series primary inductance, however starts at a negative value as opposed to zero. The current will increase to a DC level equal to the output current divided by the turns ratio, Iout/N. The two time variant contributors to primary current are the magnetizing current (Imag) and the output inductor magnetizing contribution reflected to the primary, Lout/N^2. The exact switch ON time is a function of Vin, Vout and N the transformer turns ratio, just as with conventional converters.

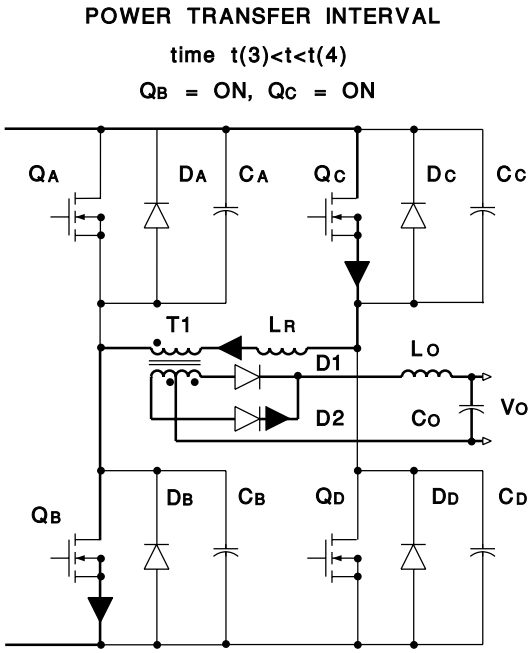


**Figure 13**

### SWITCH TURN OFF; TIME t(4)

One switching cycle is concluded at time t(4) when QC the upper right hand corner switch is turned OFF. Current stops flowing in QC's semiconductor channel but continues through the parasitic output capacitance, Coss. This increases the drain-to-source voltage from essentially zero to the full input supply voltage, Vin. The output capacitance of the lower switch in the left hand leg (QD) is simultaneously discharged via the primary current. Transistor QD is then optimally positioned for zero voltage switching with no drain-to-source voltage.

The current during this interval is assumed to be constant, simplifying the analysis. In actuality, it is slightly resonant as mentioned in the right leg transition, but the amplitude is negligible in comparison to the full load current. The power conversion interval is concluded at this point and an identical analysis occurs as for the opposite diagonal switch set which has thoroughly been described for the switch set QA and QD.

### OPERATIONAL WAVE FORMS

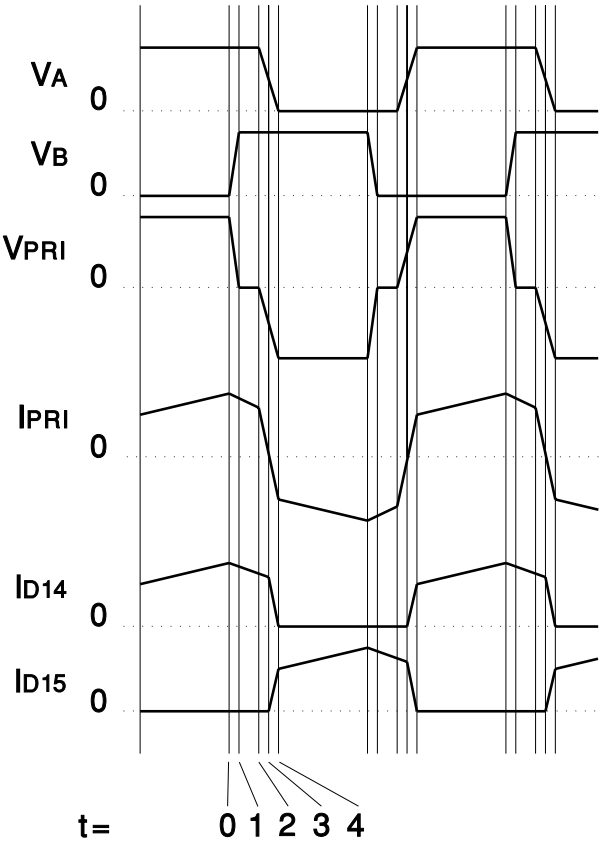


**Figure 14**

### RESONANT TANK CONSIDERATIONS

The design of the resonant tank begins with the selection of an acceptable switching frequency; one selected to meet the required power density. Second, the maximum transition time must also be established based on achievable duty cycles under all operating conditions. Experience may provide the best insight for acceptable results.

**The maximum transition time will occur during the converters left leg transition operating at the minimum output load current.**

### RESONANT CIRCUIT LIMITATIONS

*Two conditions must be met by the resonant circuit at light load, and both relate to the energy stored in the resonant inductor. One, there must be enough inductive energy stored to drive the resonant capacitors to the opposite supply rail. Two, this transition must be accomplished within the allocated transition time. Lossy, non-zero voltage switching will result if either, or both are violated. The first condition will always be met when the latter is used as the resonant circuit limitation.*

Designers can argue that some switching loss may be of little consequence in a practical application at very light loads - especially considering that there is a significant benefit at heavy loads. While this may be a pragmatic approach in many applications, and a valid concern, this presentation will continue using the fully lossless mode as the ultimate design goal.

The stored inductive energy requirement and specified maximum transition time have also defined the resonant frequency (Wr) of the tank circuit. Elements of this tank are the the resonant inductor (Lr) and capacitor (Cr), formed by the two switch output capacitors, also in parallel with the transformer primary capacitance Cxfmr. The maximum transition time cannot exceed one-fourth of the self resonant period, (four times the self resonant frequency) to satisfy the zero voltage switching condition.

The resonant tank frequency, Wr :

$$Wr = \frac{1}{(Lr \times Cr)\ \hat{}\ 0.5}$$

$$t(max)\ transition = \frac{\pi}{2 \times Wr}$$

Coss, the specified MOSFET switch output capacitance will be multiplied by a 4/3 factor to accommodate the increase caused by high voltage operation. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to 8/3 * Coss. Transformer capacitance (Cxfmr) must also be added as it is **NOT** negligible in many high frequency applications.

The resonant capacitance, Cr :

$$Cr = [\,(\frac{8}{3}\,C_{oss)+}\,Cxfmr\,]$$

The capacitive energy required to complete the transition , W(Cr) is:

$$W(\,Cr\,) = \frac{1}{2} \times Cr \times VPri\text{^}2$$

This energy can also be expressed as:

$$W(\,Cr\,) = [\,(\frac{4}{3} \times Coss) + Cxfmr\,] \times Vin\text{^}2$$

## STORED INDUCTIVE ENERGY

The energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output and transformer capacitances of the leg in transition within the maximum transition time.

Inside the transformer, all of the energy is stored in the leakage inductance since the secondary current has clamped the transformers primary voltage to essentially zero. This causes high circulating primary current (as shown in figure 8) in the physical winding but has no effect on the stored energy used to perform the ZVS transition. More detail about the tradeoffs and design optimization is presented in the Design Procedure.

The energy stored in the resonant inductor, Lr:

$$W(Lr) = \frac{1}{2}\,x\,Lr\,x\,Ipri\text{^}2$$

## RESONANT CIRCUIT SUMMARY

There are several ways to arrive at the solutions for the resonant inductor value and minimum primary current required for any application. Each of these is based upon the following fundamental relationships.

The resonant tank frequency must be at least four times higher than the transition time to fully resonate within the maximum transition time t(max) at light load.

$$Tres = 4 \times t(\,\max\,)$$

$$Fres = \frac{1}{T(\,res\,)}\;or$$

$$where\;\; Wr = 2 \times \pi \times Fres$$

$$Wr = \frac{2 \times \pi}{T(\,res\,)}$$

Reorganizing and combining these relationships;

$$Wr = \left[\frac{(\,2 \times \pi\,)}{(\,4 \times t(\,\max\,)\,)}\right]$$

$$Wr = \frac{\pi}{(\,2 \times t(\,\max\,)\,)}$$

The resonant radian frequency (Wr) is related to the resonant components by the equation:

$$Wr = \frac{1}{(\,Lr \times Cr\,)\text{^}2}$$

Both sides of this can be squared to simplify the calculations and reorganized to solve for the exact resonant inductor value.

$$Lr = \frac{1}{(\,Wr\text{^}2 \times Cr\,)}$$

Previously outlined relationships for Wr and Cr can be introduced to result in the following specific equation.

$$Lr = \frac{1}{\left[\frac{\pi}{(2 \times t(\,\max\,)}\right]\text{^}2 \times \left[(\frac{8}{3} \times Coss) + Cxfmr\right]}$$

*Note that this figure indicates the exact resonant inductor value required to satisfy only the task of resonant transitions. This resonant inductor is in series with the transformer primary hence also defines the maximum primary current slew rate, dI/dt as a function of input voltage.*

$$\frac{d\,IPri}{dt} = \frac{Vin}{Lr}$$

If the resonant inductor value is too large it may take too long to reach the necessary load current within the conversion cycle. The calculated inductor value satisfies the light load condition, however full load operation must also be evaluated. Details of possible solutions to this are highlighted in the Practical Applications section of this paper.

## STORED ENERGY REQUIREMENTS

As detailed, the energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. The governing equations are summarized below.

$$\frac{1}{2} \times Lr \times IPri(\,\min\,)\text{^}2 \;>\; \frac{1}{2} \times Cr \times Vin(\,\max\,)\text{^}2,\; or$$

$$Lr \times IPri(min)\text{^}2 \;>\; Cr \times Vin(\,\max\,)\text{^}2$$

Since Cr and Vin are known or can be estimated for a given application, this term becomes a constant and Lr has been quantified.

## MINIMUM PRIMARY CURRENT

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation.

$$IPri(\min) = \left[\frac{(Cr \times Vin\text{^}2)}{Lr}\right]\text{^}0.5$$

This value can be supported by the calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower that IP(min) it can be used as a confirmation of the mathematics.

$$IR(average) = Cr \times \frac{Vin}{t(\max)}$$

Obtaining the necessary amount of primary current can be done in several ways. The most direct approach is to simply limit the minimum load current to the appropriate level. One alternative, however, is to design the transformer magnetizing inductance accordingly. Also assisting the magnetizing current is the reflected secondary inductor current contribution which is modeled in parallel. Any duty cycle variations modifying the peak charging current must also be taken into account.

Generally the magnetizing current alone is insufficient in many off-line high frequency converters. The transformer is usually cores loss limited which means numerous primary turns and a high magnetizing inductance. Shunting the transformer primary with an external inductor to develop the right amount of primary current is one possibility. Incorporating the output filter inductor magnetizing current to assist resonance on the primary side is also an alternative.

## PHASE SHIFTED PWM CONTROL CIRCUITRY

Probably the most critical control aspect in the phase shifted PWM technique is the ability to span the full 0 to 180 degree phase shift range. Falling short of performance on either end of the spectrum can place unnecessary burdens on the fault protection circuitry or primary switches. Loss of control at either extreme will result in catastrophic consequences by simultaneously turning on both transistors in a given “leg” of the converter. The UC3875 Phase Shifted controller features the required circuitry to deliver both zero and effectively full duty cycle - effortlessly. Additionally, the UC3875 controller is utilized to perform the necessary control, decoding, protection and drive functions for this application. Peak current mode control is implemented for this example although the IC is equally suited for conventional voltage mode control, with or without input voltage feed forward. When used in current mode, the IC accepts a zero to 2.7 volt amplitude maximum current senses input and makes adding slope compensation a simple function.

**UC3875 Block Diagram**

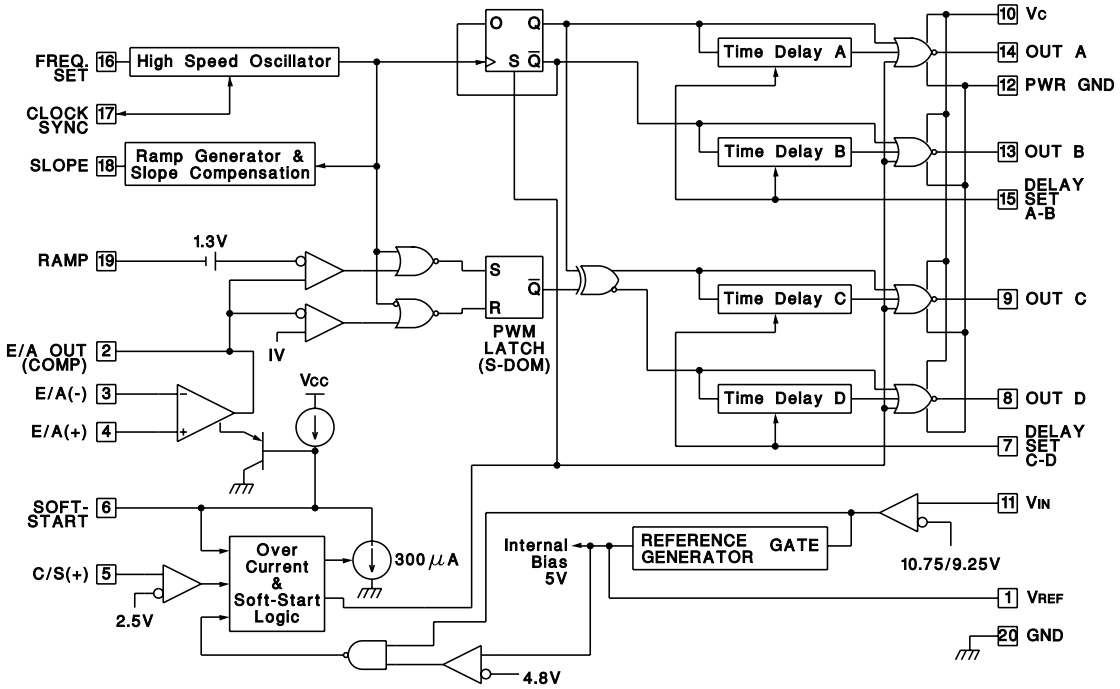


**Figure 16**

## UNITRODE UC3875 PHASE SHIFTED PWM CONTROL IC - BLOCK DIAGRAM

A synchronizable oscillator is programmed by a resistor capacitor network from the frequency set pin to ground. Synchronization is performed by driving the SYNC pin from another UC3875 or external circuitry. The precision 5.0 volt bandgap reference is available to program the noninverting input of the error amplifier as well as optional external functions. Output regulation is achieved using the 7 MHz gain-band width on-board error amplifier which feeds the high speed PWM circuitry. Soft starting is accomplished with a capacitor to ground which gradually increases the error amplifier output, corresponding to pulse width, phase shift or peak current, depending on the exact implementation. This signal is compared to the Ramp input of the IC having a usable input range from zero to 2.7 volts.

Delays between the output drive commands to facilitate Zero Voltage Switching are programmed at the Delay Set inputs. One unique feature of the UC3875 is the ability to separately program the A-B output delays differently from the C-D outputs. This capability accommodates the different primary currents during one switching cycle which cause and result in different resonant transition times between the leading and falling edges. Inability to program each of these durations will generally result in lossy, non-zero voltage switching of the full bridge converters switches under some operating conditions.

The four UC3875 output totem poles can each deliver a two amp peak gate drive current, more than adequate in a high frequency transformer coupled gate drive application. To minimize noise transmitted back to the analog circuitry, the output section features its own collector power supply (Vc) and ground (PGND) connections. Local decoupling capacitors and series impedance to the auxiliary supply further enhances performance.

Fault protection is established by the programmable current limit circuitry. Full cycle restart corresponding to the time programmed by the soft start interval minimizes power dissipation in a short circuited output.

## TYPICAL APPLICATION CIRCUIT SCHEMATIC SUMMARY

The fixed frequency phase shifted control technique of the full bridge converter offers numerous performance advantages over the conventional approach. switching losses due to the simultaneous overlapof voltage and current disappear along with the dissipative discharge of the FET output capacitance. EMI/RFI is significantly lower, also due to the "soft" switching characteristics which incorporate parasitic elements of the power stage acvantageously. For most applications, there is little reason to consider the traditional square wave counterpart of theis phase shifted PWM technique for future designs.

Very high frequency operation of this technique, beyond 500 KHz, is probable above the optimal operating point. Transition times quickly erode the usable duty cycle to a point where the transformer turns ratio has been compromised. This could result in unreasonably high primary currents and repower loss in the switches. Any incremental gains in cost or power density by reducting the size of the output filter are probably nullified by the needs for larger MOSFETs and heatsinks. This phase shifted PWM technique does excel in the overall majority of mid to high power, off-line applications. Peak efficiency will be obtained in applications with moderate load ranges, however excellent results can also be obtained in most designs with load ranges of ten-to one. A subgroup of applications may exist where non ZVS operation extremely light loads is acceptable, especially when the advantages under all other operating conditions are considered. Additionally, the Unitrode UC3875 Phase Shifted Controlller IC has been introduced to simplify the control circuit design challenge. Features of the UC3875 include 2 MHz operation and four 2 amp peak totem-pole output drivers for high frequency applications. Separate programming of the different AD and BC leg transition intervals has made available to optimize converter performance.

Finally, the flexible control logic permits current mode or voltage mode control, with or without input voltage feed forward. The complexity of control, drive and protection of the fixed frequency phase shifted converter has been fully addressed in a single integrated solution.

**UC3875 Phase Shifted PWM Converter**
**Control and Output Circuit Schematic**

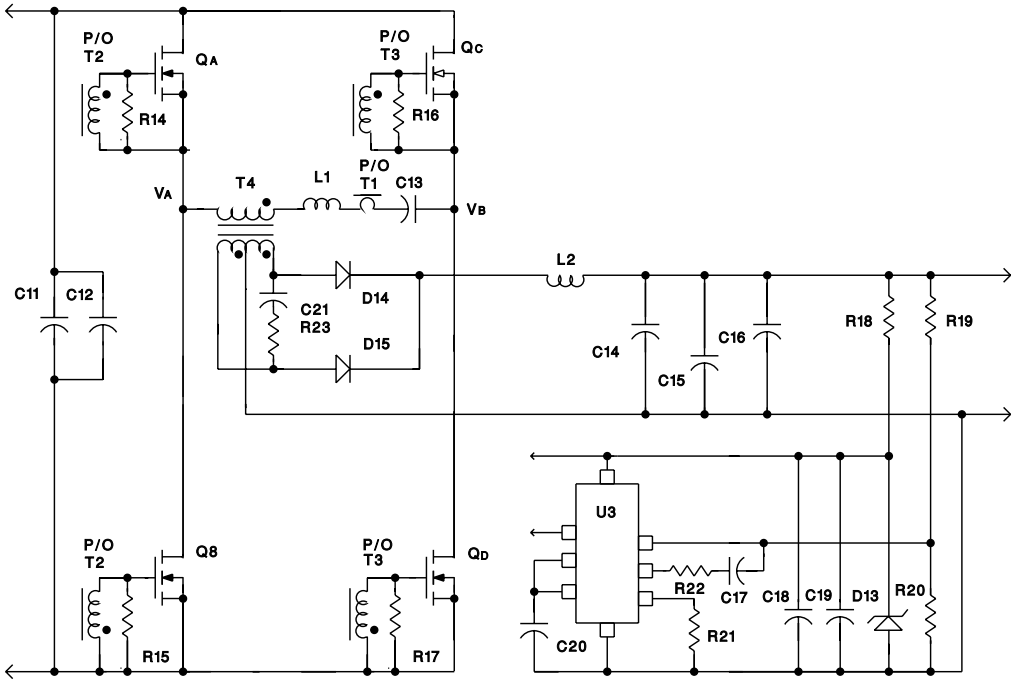


**Figure 17**

**UC 3875 Phase Shifted PWM Converter**
**Control and Drive Circuit Schematic**

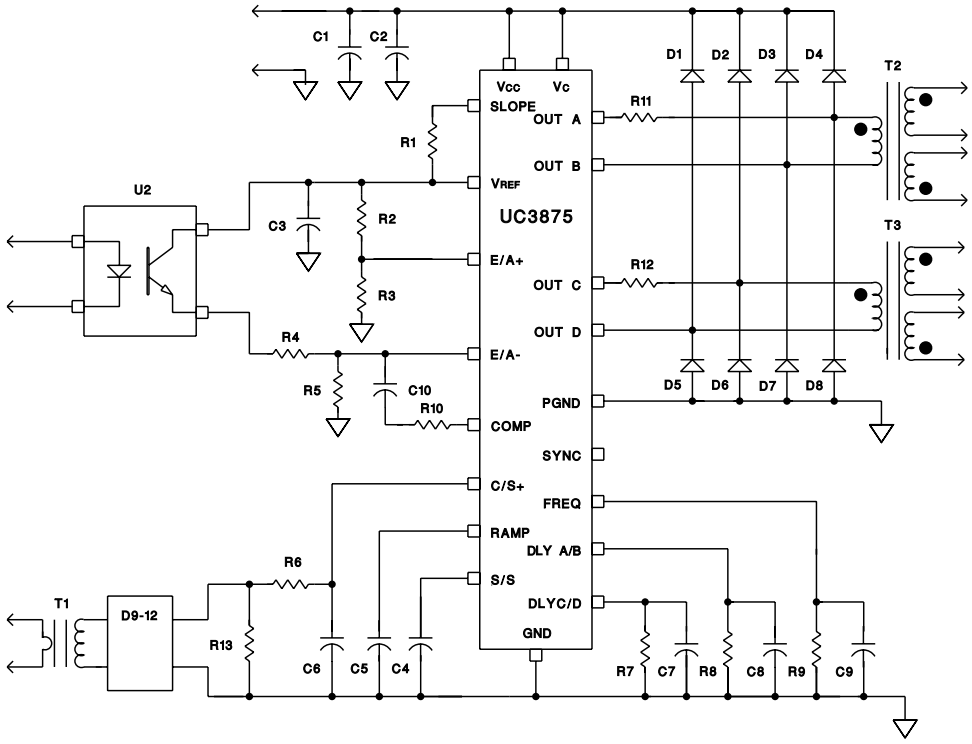


**Figure 18**

UC3875 F.B.P.S. CONVERTER

LIST OF MATERIALS

CAPACITORS

All are 20 VDC Ceramic Monolithic or Multilayer UNLESS "*" indicated.

C1= 1 μF
C2= 47 μF/25V ELECTROLYTIC
C3= 1 μF
C4= 1 μF
C5= 75 pF/16V POLYSTYRENE
C6= 0.001 μF
C7, 8= 0.01 μF
C9= 470 pF
C10= 0.1 μF
C11= 1 μF/450VDC POLY
C12= 47μ/450VDC ELECTROLYTIC
C13= 1.2μF/450 VDC POLY
C14= 1μF/100VDC
C15, 16= 220μF/63VDC ELECTROLITIC
C17= TBD
C18= 1μF
C19= 22 μF/25VDC ELECTROLITIC
C20= 1 μF
C21= 2.7 nF/200V POLY/low ESL&ESR

DIODES
D1-8= 1N5820 3A/20V SCHOTTKY
D9-12= 1N4148
D13= 12V 3W ZENER
D14, 15= 15A/200V FAST RECOVERY

INDUCTORS
L1= 47μH/3A
L2= 100μH/15A

MOSFET TRANSISTORS
QA-D=IRF840 NMOS

Bill Andreycak / UICC
2/24/93

RESISTORS

All are 1/2 Watt, 1%, Metal Film UNLESS "*" indicated

R1= 75K
R2= 2K
R3= 3K
R4= 470 Ohm
R5= 3K
R6= 100 Ohm
R7, 8= 6.8K
R9= 43K
R10= 150K
R11, 12= 10 Ohm
R13= 20 Ohm
R14-17= 10K
R18= 3.6K, 1WATT
R19= 36K
R20= 1K
R21= TBD
R22= TBD
R23= 110 Ohms/5W Carbon

TRANSFORMER
T1= 1 SENSE
T2, 3= GATE DRIVERS
T4= MAIN XFMR

INTEGRATED CIRCUITS
U1= UC3875 PMW
U2= OPTO
U3= UC19432

**One Switching Cycle**

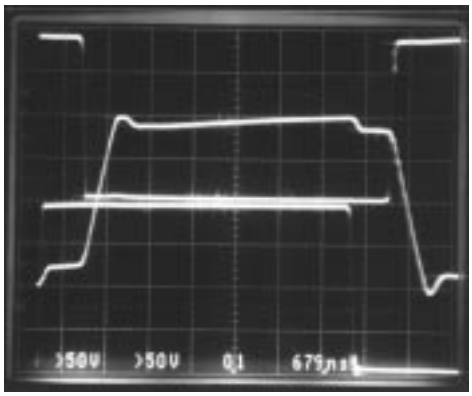


**Figure 19**

**Primary Waveforms**

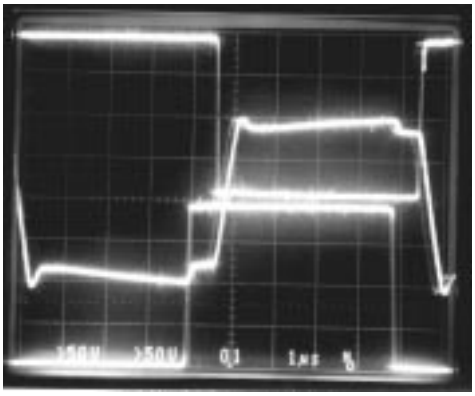


**Figure 20**

**Secondary Waveforms**

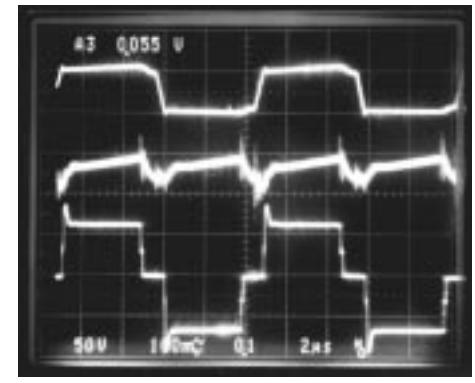


**Figure 21**

## REFERENCES

1. STEIGERWALD, R. and NGO, K; “Full Bridge Lossless Switching Converter”; United States Patent #4,864,479

2. DALAL, D.; “A 500 KHz Multi-Output Converter rogrammed by theft start interval minimizes power dissipation in twith Zero Voltage Switching”; IEEE 1990

3. FISHER, NGO and KUO; “A 500 KHz, 250 W DC-DC Converter with Multiple Outputs COntrolled by Phase SHifted PWM and Magnetic Amplifiers ” HFPC 1988"; HFPC 1988

4. ANDREYCAK, W. “Zero Voltage Switching Resonant Power Conversion”; UNITRODE Power Supply Design Seminar SEM-700, 1990

5. MWEENE, WRIGHT and SCHLECHT, “A 1 KW, 500 KHz Front-End Converter for a Distributed Power Supply System”; IEEE 1989

6. ANDREYCAK, W. “Controlling Zero Voltage Switched Power Supplies”; HFPC Proceedings 1990

7. SABATE′, VLATKOVIC′, RIDLEY, LEE and CHO; “Design Considerations for High Voltage, High Power, Full Bridge, Zero Voltage Switched PWM Converter; IEEE APEC 1990

8. LOFTI, SABATE′, and LEE; “Design Optimization of the Zero VOltage Switched PWM Converter”; VPEC Seminar 1990

9. CHEN, LOFTI and LEE; “Design Tradeoffs in 5V Output Off-line ZVS PWM Converters”; Proceedings of the International Telecommunications Energy Conference; Kyoto, Japan 1991

## ACKNOWLEDGMENTS

This Application Note is an edited version of a paper presented at the **1992 High Frequency Power Conference** sponsored by **Intertec Communications** and was first published in the Conference Proceedings.

The author acknowledges and appreciates the assistance of **John A. O’Connor** during the course of this project.

The works of the individuals listed in the references including **Dr. Fred Lee** from **Virginia Power Electronics Center at Virginia Tech.** are applauded.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.